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TEXAS
INSTRUMENTS



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• HBT Process Development

Two ADC lots completed processing during May. These lots, the second and third completed ADC lots, exhibit low transistor gains similar to the first lot, although one slice from the third lot does exhibit gains greater than 50 and could result in potentially good ADC circuits. Figure 1 shows the I-V curves of one of the $7 \times 7 \mu\text{m}^2$ transistors fabricated on this good wafer. The dc current gain was 100 at low current and 1000 at high current. These gain values were obtained over one chip, but started decreasing in adjacent chips. A 19-stage HECL ring oscillator fabricated on this wafer and designed with the $7 \times 7 \mu\text{m}^2$ emitter HBT and differential interstage coupling gave switching speeds of 87 ps/gate at 27 mW/gate (see Figure 2). This result validates the potential of the overgrowth process while indicating much work still needs to be done on uniformity and yield. The third lot has been shipped to Hughes along with the dc multiprobe wafer maps for testing of the ADCs and sample-and-hold circuits.

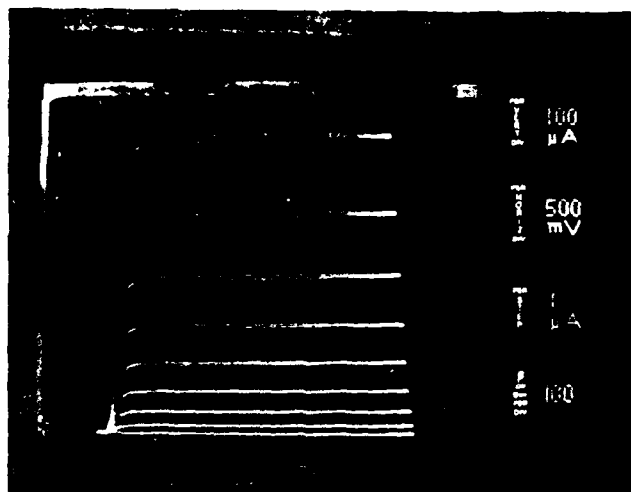
One yield problem that has been addressed during the past few months is the unintentional formation of a Schottky diode between the base and emitter contact, resulting in low V_{be} and low gain. The emitter ohmic metal is usually slightly misaligned to the ohmic cap etch pattern. Consequently, while the AuGe/Ni resides mostly on the GaAs cap layer, some of the metal is beyond the edge of the GaAs cap and on the AlGaAs emitter layer. If the AuGeNi penetrates too far through the emitter layer during the alloy, then a

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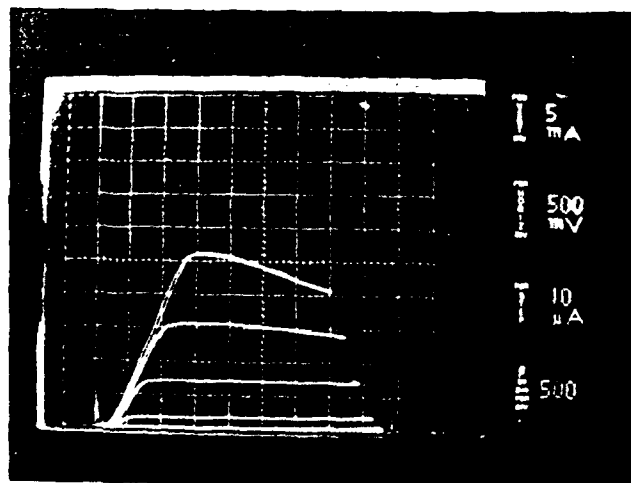
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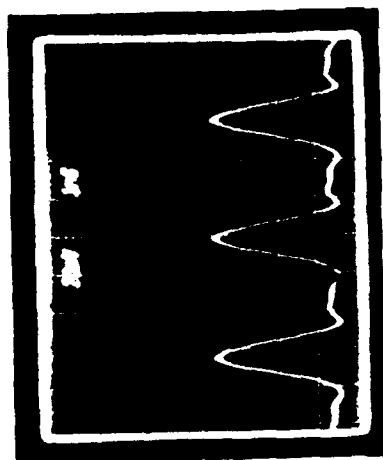
Low Current

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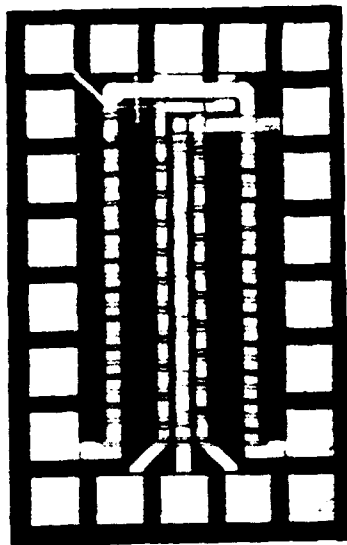


High Current

Figure 1. I-V characteristics for npn HBT from ADC Lot 3.



87 ps GATE DELAY



19-STAGE RING OSCILLATOR

Figure 2. 19-Stage GaAs HECL ring oscillator.

Schottky diode can occur between the metal and the base. To eliminate this problem, a self-aligned side-wall nitride process has been developed. A side-wall of nitride will be formed around the n-ohmic and p-ohmic metal to protect the metal/GaAs interface from attack during the etch of the GaAs cap layer, which will now be done after ohmic contact formation. This new process has just been initiated, and results will be evaluated in a few months, after several lots have undergone the new process.

- N-Channel JFET Process Development

One of the advantages of TI's HBT process is the integration of npn HBTs and n-channel JFETs for improved circuit performance. Most of the effort during the past year has addressed the npn devices. As we begin to improve the npn HBTs, more effort will be shifted toward the JFETs. The initial process demonstrating the successful integration of the npn HBTs and n-JFETs utilized a thin p-epi layer grown over the top on the npn emitter layers and selectively etched from the surface except in the JFET gate regions and p-ohmic contact regions. The use of a grown p-epi layer for the n-JFET gate is being reexamined. When the p-epi is doped to $1 \times 10^{19}/\text{cm}^3$, the Zn diffusion out of the layer and into the n-AlGaAs, at $2 \times 10^{17}/\text{cm}^3$, can destroy the channel. While p-type epi layers doped to $1 \times 10^{18}/\text{cm}^3$ may minimize this problem, an alternative process utilizing BeCl implants will be explored. The atomic mass of the BeCl molecule is 44, compared to 9 for Be. The result is a very shallow Be implant profile.

The calculated doping profile of the BeCl implant is shown in Figure 3 integrated into a JFET cross section. It can be seen that the peak doping of $2 \times 10^{19}/\text{cm}^3$ occurs within a range of 1000 Å, which makes conversion of the highly doped n-type cap layer easy. The channel for the n-JFET is then defined between a base layer and the gate, which includes the npn AlGaAs emitter. Also shown for comparison is a similar fluence Be implant. It is clear that the BeCl implant has the potential for very shallow p-type gate regions on the n-JFET, as well as shallower npn vertical dimensions and hence faster devices. The BeCl implant is a powerful new tool for doping GaAs. BeCl has also been used to form the channel for p-JFET in a first epi material on which a gate of n-AlGaAs was subsequently grown, allowing the integration of npn HBTs and p-JFETs. BeCl has also been used for the base

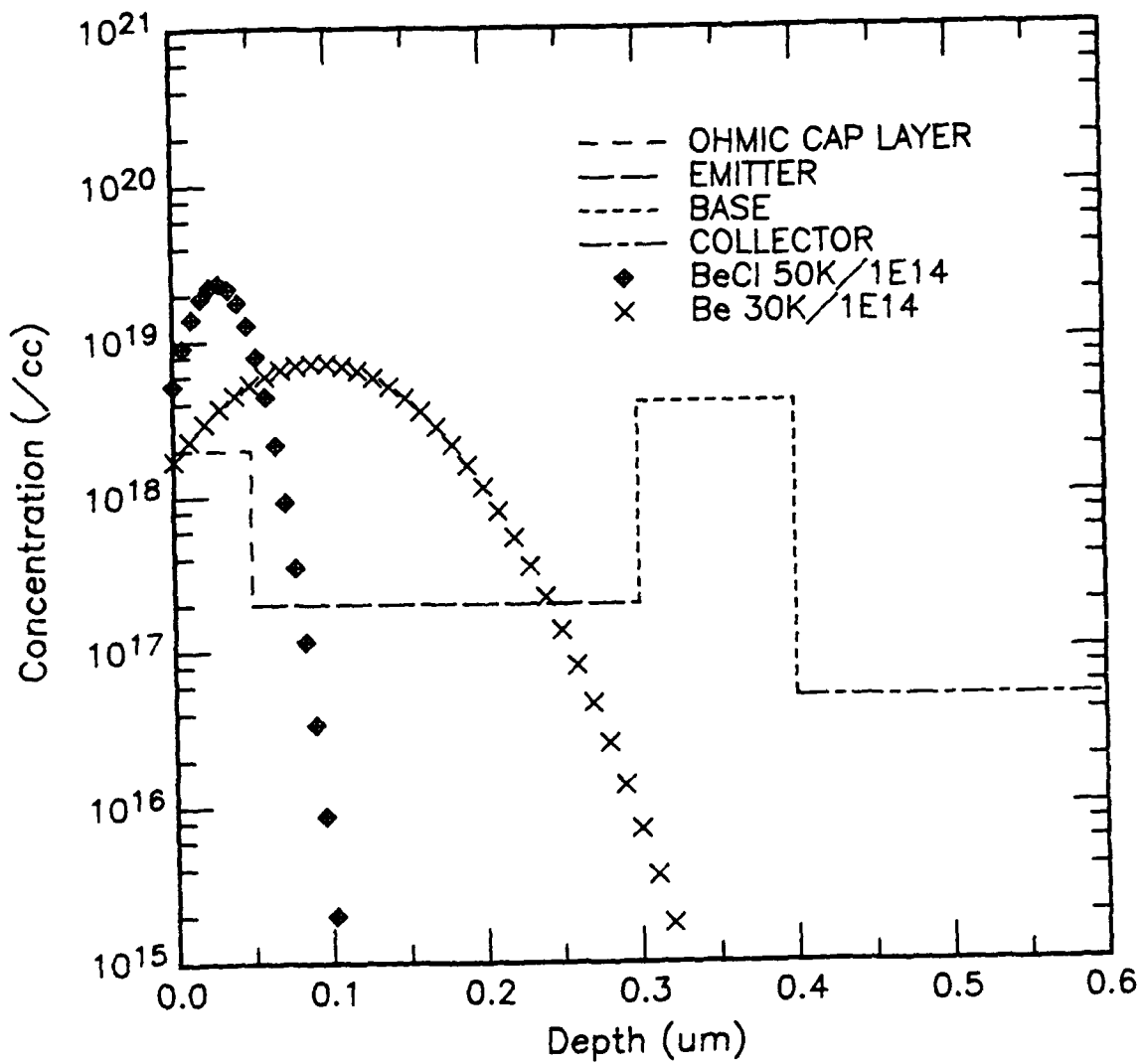


Figure 3. n-JFET gate formation in npn epi.

implant in the overgrowth process, which has resulted in transistors with gains of 5 to 20, depending on the implant fluence. The uniformity of these results is being checked; however, it is hoped that the diffusion of the Be dopant will be easier to control than that of Zn. Clearly, a BeCl implant profile such as that shown in Figure 3 for the gate can give a good base doping profile with a width less than 1000 Å. The effects of the Cl on the Be activation have yet to be characterized. Because of the shallow nature of the implant and the possible effects of the Cl, the dose of the implant will have to be carefully cross-referenced to the anneal cycle.

- Circuit Design Progress

A detailed architecture study for the 1.5 Gsps, 8-bit ADC design continued during May. The optimum 8-bit quantizer folding and interpolation architecture was identified. Among the critical design factors that were considered were optimum dc linearity and temperature stability, input signal distribution, required decoding circuitry, and layout factors.

Detailed circuit simulation of the 8-bit ADC cannot be completed until an accurate model for the overgrowth HBT transistor can be established. Accurate modeling of device parameters, including β , junction breakdown voltages and capacitances, and f_T , is required for simulation results to be meaningful. In addition, accurate statistical information concerning V_{be} and β matching is critical for circuit design optimization. As a result, progress toward completion of the 8-bit ADC mask set is expected to be delayed until an HBT process with stable β and reasonable yield can be established. A corresponding slip in the release of the 8-bit and 12-bit mask sets is expected.

- Device Characterization

Modeling efforts are on hold until a representative overgrowth lot is received.

- Personnel Assignments

There have been no changes in personnel.

- Plans

TI will:

- Run special tests to isolate low current gain problems
- Continue electrical characterization of the completed lots
- Continue overgrowth process development.

Hughes will:


- Complete wafer-level testing of the second test-bar lot expected from TI at the beginning of the month and verify 5-bit ADC design
- Dynamically evaluate any functional 5-bit ADC and S/H circuits from the June lot
- Initiate detailed characterization of HBT devices from the June lot, if representative of processing goals
- Initiate detailed design of 8-bit ADC if HBT process with stable β is established.

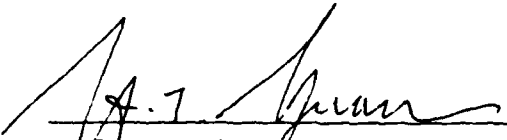
- Unofficial DARPA Financial Status Report


This is the financial status as of 31 May 1988:

	Funds <u>Authorized</u>	Funds <u>Spent</u>	Amount <u>Billed</u>	Amount <u>Received</u>
FY88	\$1,330,000	\$1,032,967	\$957,967	\$866,467

Contract Number: N00014-87-C-0314
 Contract Title: GaAs Heterojunction Device Based A/D
 Start Date: 03/30/87


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